Energy Conversion and Management 50 (2009) 2761–2767

Contents lists available at ScienceDirect

Energy Conversion and Management

journal homepage: www.elsevier.com/locate/enconman

New cascaded multilevel inverter topology with minimum number of switches

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ARTICLE INFO

Article history:
Received 29 November 2008
Accepted 29 June 2009
Available online 28 July 2009

Keywords:
Multilevel inverter
Cascaded multilevel inverter
Sub-multilevel inverter
Full-bridge
H-bridge

ABSTRACT

In this paper, a new topology of cascaded multilevel inverter using a reduced number of switches, insulated gate driver circuits and voltage standing on switches is proposed. The proposed topology results in reduction of installation area and cost and has simplicity of control system. This structure consists of series connected sub-multilevel inverters blocks. Three algorithms for determination of magnitudes of dc voltage sources have been presented, too. Validity of the analysis has been proved by simulation and experimental results.

1. Introduction

A multilevel inverter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. Recently, multilevel power conversion technology has been developing the area of power electronics very rapidly with good potential for further developments. The most attractive applications of this technology are in the medium to high voltage ranges.

The concept of utilizing multiple small voltage levels to perform power conversion was presented by a MIT researcher [1,2]. Advantages of this multilevel approach include good power quality, good electro-magnetic compatibility, low switching losses and high voltage capability.

The first introduced topology is the series H-bridge design [1]. This was followed by the diode-clamped inverter [2–4] which utilizes a bank of series capacitors to split the dc bus voltage. The flying-capacitor (or capacitor clamped) [5] topology followed diode-clamped after few years, instead of series connected capacitors, this topology uses floating capacitors to clamp the voltage levels. Another multilevel design, slightly different from the previous one, involves parallel connection of inverter phases through interphase reactors [6]. In this design the semiconductors must block the entire voltage, but share the load current. Also, several combinatorial designs have emerged [7], implemented cascading the fundamental topologies [8–12]; they are called hybrid topologies. These designs can create power quality for a given number of semiconductor devices higher than the fundamental topologies alone due to a multiplying effect of the number of levels [13]. Also, some soft-switching methods can be implemented for different multilevel inverters to reduce the switching loss and to increase efficiency [14,15]. Recently, several multilevel inverter topologies have been developed [16–19].

Unfortunately, multilevel inverters have some disadvantages. One particular disadvantage is the great number of power semiconductor switches needed. Although low voltage rate switches can be utilized in a multilevel inverter, each switch requires a related gate driver circuits. This may cause the overall system to be more expensive and complex. So, in practical implementation, reducing the number of switches and gate driver circuits is very important.

This paper suggests a new topology for cascaded multilevel inverters with a high number of steps associated with a low number of switches and gate driver circuits for switches. In addition, for producing all levels (odd and even) at the output voltage, three procedures for calculating the required dc voltage sources are proposed. Finally, the paper includes simulation and experimental results to prove the feasibility of the proposed multilevel inverter.

2. Conventional cascaded multilevel inverters

The full-bridge topology with four switches is used to synthesize a three-level square-wave output voltage waveform. The cascaded multilevel inverter consists of series connections of n full-bridge topology. Fig. 1 shows the configuration of cascaded multilevel inverter. The overall output voltage of multilevel inverter is given by:

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doi:10.1016/j.enconman.2009.06.032

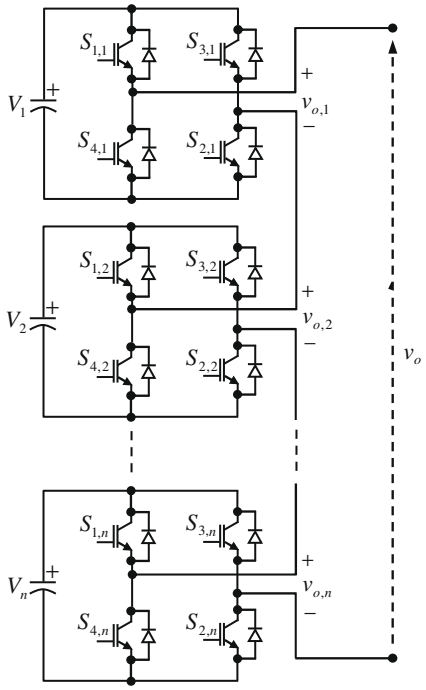


Fig. 1. Configuration of cascaded multilevel inverter.

$$v_o = v_{o,1} + v_{o,2} + \cdots + v_{o,n} \tag{1}$$

If all dc voltage sources in Fig. 1 equal to V_{dc}, the inverter is known as symmetric multilevel inverter. The effective number of output voltage steps (N_{step}) in symmetric multilevel inverter may be related to the number of full-bridges (n) by:

$$N_{step} = 2n + 1 \tag{2}$$

and the maximum output voltage ($V_{o,max}$) of this n cascaded multilevel inverter is:

$$V_{o,max} = n \times V_{dc} \tag{3}$$

To provide a large number of output steps without increasing the number of inverters, asymmetric multilevel inverters can be used. In [20,21], the dc voltages sources are proposed to be chosen according to a geometric progression with a factor of two or three. For n cascaded multilevel inverters, the number of voltage steps is given as follows:

$$N_{step} = 2^{n+1} - 1 \quad \text{if } V_j = 2^{j-1}V_{dc} \quad \text{for } j = 1, 2, \ldots, n \tag{4}$$

$$N_{step} = 3^n \quad \text{if } V_j = 3^{j-1}V_{dc} \quad \text{for } j = 1, 2, \ldots, n \tag{5}$$

The maximum output voltages of these n cascaded multilevel inverters are:

$$V_{o,max} = (2^n - 1)V_{dc} \quad \text{if } V_j = 2^{j-1}V_{dc} \quad \text{for } j = 1, 2, \ldots, n \tag{6}$$

$$V_{o,max} = \left(\frac{3^n - 1}{2}\right)V_{dc} \quad \text{if } V_j = 3^{j-1}V_{dc} \quad \text{for } j = 1, 2, \ldots, n \tag{7}$$

Comparing the Eqs. (2)–(7), it can be seen that the asymmetric multilevel inverters can generate more voltage steps and higher maximum output voltage with the same number of bridges.

3. Suggested topology

Fig. 2 shows the suggested basic unit for a sub-multilevel inverter. This consists of a capacitor (with dc voltage equal to V_{dc}) with two switches S_1 and S_2. Table 1 indicates the values of v_o for states of switches S_1 and S_2. It is clear that both switches S_1 and S_2 can not

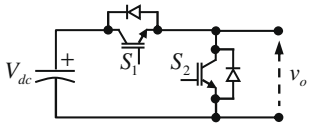


Fig. 2. Suggested basic unit for a sub-multilevel inverter.

Table 1
Values of v_o for states of switches S_1 and S_2.

State	Switches states		v_o
	S_1	S_2	
1	On	Off	V_{dc}
2	Off	On	0

be on simultaneously because a short circuit across the voltage V_{dc} would be produced. It is noted that two values can be achieved for v_o. The basic unit shown in Fig. 2 can be cascaded as shown in Fig. 3.

Although this topology requires multiple dc sources, in some systems they may be available through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices such as capacitors or batteries. When ac voltage is already available, multiple dc sources can be generated using isolated transformers and rectifiers [22].

The overall output voltage of the suggested cascaded multilevel inverter is given by Eq. (1). Table 2 shows the values of v_o for state of switches $S_1, S_2, \ldots, S_{2n-1}, S_{2n}$. As can be seen, 2^n different values can be obtained for v_o. Fig. 4 shows a 5-level typical output

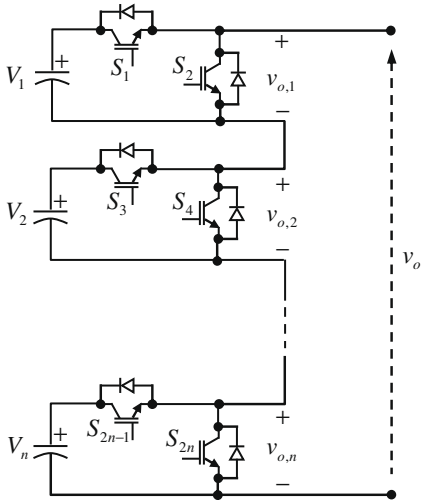


Fig. 3. Cascaded basic units.

Table 2
Values of v_o for state of switches.

State	Switches states							v_0
	S_1	S_2	S_3	S_4	$\cdots$	S_{2n-1}	S_{2n}	
1	Off	On	Off	On	$\cdots$	Off	On	0
2	On	Off	Off	On	$\cdots$	Off	On	v_1
3	Off	On	On	Off	$\cdots$	Off	On	v_2
4	On	Off	On	Off	$\cdots$	Off	On	$V_1 + V_2$
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\vdots$	$\vdots$
2^n	On	Off	On	Off	$\cdots$	On	Off	$\sum_{i=1}^{n} v_1$

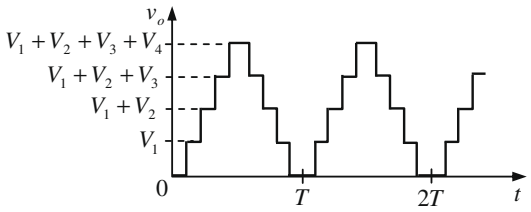


Fig. 4. Typical output waveform of 5-level.

waveform of the proposed multilevel inverter. As this figure shows, the output voltage for all times has zero or positive value.

In the following, we propose three different methods for determination of magnitudes of dc voltage sources which are used in the proposed multilevel inverter. It is worth noting that by all proposed methods, every number of output voltage steps (even and odd) can be produced.

3.1. First method

If all dc voltage sources in Fig. 3 equal to V_{dc}, the inverter is then known as symmetric multilevel inverter. The number of maximum output voltage steps of the n series basic units can be evaluated by:

$$N_{step} = n + 1 \tag{8}$$

The reason for using the term "maximum" is that it is possible to have an equal value for v_o over different states of the switches. The maximum output voltage is given by:

$$V_{o,max} = n \times V_{dc} \tag{9}$$

3.2. Second method

The second method for determination of the magnitudes of dc voltage sources is in binary fashion which gives an exponential increasing in the number of the overall output levels. For n series basic units, with dc voltage levels varying in binary fashion, the number of maximum output voltage steps and maximum output voltage are calculated by Eqs. (10) and (6), respectively.

$$N_{step} = 2^n \tag{10}$$

3.3. Third method

In the third method, the dc voltage sources in the proposed multilevel inverters are suggested to be chosen according to the following equations:

$$V_1 = V_{dc} \tag{11}$$

$$V_j = 2V_{dc} \quad \text{for } j = 2, 3, 4, \ldots, n \tag{12}$$

The number of maximum output voltage steps can be determined by the following equation:

$$N_{step} = 2n \tag{13}$$

The maximum output voltage of this n cascaded multilevel inverter is:

$$V_{o,max} = (2n-1)V_{dc} \tag{14}$$

4. Extended structure

The multilevel proposed in Fig. 3, only can generate the positive output voltages. For generating both of the positive and negative output voltages, the structure shown in Fig. 5 is proposed. In this

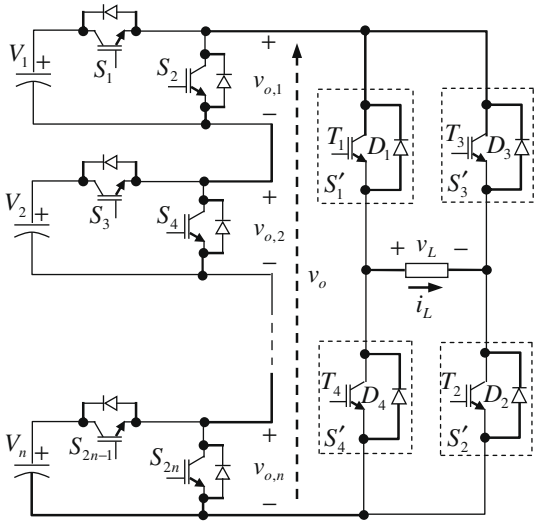


Fig. 5. The proposed structure for generating both of the positive and negative output voltages.

figure, the full-bridge topology added to the output terminals of the circuit shown in Fig. 3. The direction of load current and voltage are as shown in Fig. 5. It is clear that both switches S'_1 and S'_4 (or S'_2 and S'_3) can not be on simultaneously because a short circuit across the voltage v_o would be produced. There are four defined switch states as shown in Table 3. Fig. 6 shows a 9-level typical output waveform of the proposed multilevel inverter. The switches S'_1 and S'_2 are fired together and conduct for $0 < t < T$. At $t = T$, the switches S'_1 and S'_2 are turned off and the switches S'_3 and S'_4 are turned on. Thus S'_3 and S'_4 conduct for the duration $T < t < 2T$. For this duration, the direction of v_L is opposite to v_o as shown in

Table 3
Switches states for a full-bridge.

State	Switches states				v_L	Components conducting
	S'_1	S'_2	S'_3	S'_4		
1	On	On	Off	Off	v_o	T_1 and T_2 if $i_L > 0$ D_1 and D_2 if $i_L < 0$
2	Off	Off	On	On	$-v_o$	D_3 and D_4 if $i_L > 0$ T_3 and T_4 if $i_L < 0$
3	On	Off	On	Off	0	T_1 and D_3 if $i_L > 0$ D_1 and T_3 if $i_L < 0$
4	Off	On	Off	On	0	D_4 and T_2 if $i_L > 0$ T_4 and D_2 if $i_L < 0$

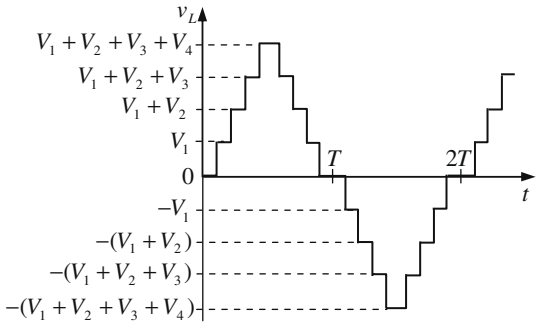


Fig. 6. Typical output waveform of 9-level.

Fig. 6 and the negative half of output waveform is obtained. Diodes D_1–D_4 act as freewheeling operation.

In the topology shown in Fig. 5, the number of maximum output voltage steps for three methods mentioned in Section 3 is given by the following equations, respectively:

First method:

$$N_{step} = 2n + 1 \tag{15}$$

Second method:

$$N_{step} = 2^{n+1} - 1 \tag{16}$$

Third method:

$$N_{step} = 4n - 1 \tag{17}$$

5. Comparison of the suggested structure with conventional cascaded multilevel inverter

The main purpose of this paper is reduction of the components of the cascaded multilevel inverters. Each switch in the suggested topology is composed of one insulated-gate bipolar transistor (IGBT) and one anti-parallel diode. Also, each switch requires one gate driver as shown in Fig. 7. Fig. 7 shows the isolator and driver circuit of each switch. This circuit consists of an opto-isolator, a schmit trigger and a buffer. Each switch in the inverter requires an isolated driver circuit. The isolation can be provided using either pulse transformers or opto-isolators. Opto-isolators can work in a wide range of input signal pulse width, but a separate isolated power supply is required for each switching device. The opto-isolator based gate driver circuit is used in prototype.

Another important problem in inverters is the ratings of switches. In other word, voltage and current ratings of the switches in a multilevel inverter play important roles on the cost and realization of the inverter. In the proposed topology, the currents of all switches are equal with the rated current of the load. This is, however, not the case for the voltage. Suppose that the peak inverse voltage (PIV) of all switches is represented by:

$$\text{PIV} = \sum_{j=1} V_{\text{switch},j} \tag{18}$$

In the above equation, $V_{\text{switch},j}$ represents the peak inverse voltage of the jth switch. Therefore, the Eq. (18) can be considered as a criterion for comparison of different topologies from the maximum

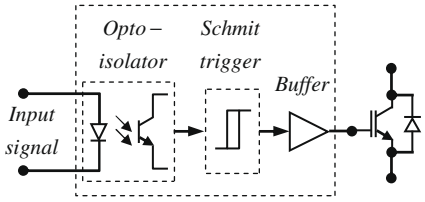


Fig. 7. Gate driver circuit for a switch.

Table 4
Comparison of power component requirements among conventional cascaded multilevel inverters.

	Symmetrical	Symmetrical	
		Binary	Trinary
Maximum output voltage	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$
Number of switches, IGBTs and gate drivers	$2(N_{step}-1)$	$4\left[\frac{\ln(N_{step}+1)}{\ln 2}-1\right]$	$\frac{4\ln N_{step}}{\ln 3}$
Number of capacitors	$\frac{N_{step}-1}{2}$	$\frac{\ln(N_{step}+1)}{\ln 2}-1$	$\frac{\ln N_{step}}{\ln 3}$
Variety of magnitudes of dc voltage sources	1	$\frac{\ln(N_{step}+1)}{\ln 2}-1$	$\frac{\ln N_{step}}{\ln 3}$
Standing voltage	$2V_{dc}(N_{step}-1)$	$2V_{dc}(N_{step}-1)$	$2V_{dc}(N_{step}-1)$

Table 5
Comparison of power component requirements for suggested multilevel inverter.

	First method	Second method	Third method
Maximum output voltage	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$	$V_{dc}\left(\frac{N_{step}-1}{2}\right)$
Number of switches, IGBTs and gate drivers	$N_{step}+3$	$\frac{2\ln[2(N_{step}+1)]}{\ln 2}$	$\frac{N_{step}+9}{2}$
Number of capacitors	$\frac{N_{step}-1}{2}$	$\frac{\ln(N_{step}+1)}{\ln 2}-1$	$\frac{N_{step}+1}{4}$
Variety of magnitudes of dc voltage sources	1	$\frac{\ln(N_{step}+1)}{\ln 2}-1$	2
Standing voltage on S_1–S_{2n}	$V_{dc}(N_{step}-1)$	$V_{dc}(N_{step}-1)$	$V_{dc}(N_{step}-1)$
Standing voltage on S'_1–S'_4	$2V_{dc}(N_{step}-1)$	$2V_{dc}(N_{step}-1)$	$2V_{dc}(N_{step}-1)$
Standing voltage on all of the switches	$3V_{dc}(N_{step}-1)$	$3V_{dc}(N_{step}-1)$	$3V_{dc}(N_{step}-1)$

voltage standing on the switches [23]. In the proposed inverter, the voltage standing on switches in Fig. 3 for the suggested three methods is given by the following equation:

$$PIV = V_{dc}(N_{step} - 1) \tag{19}$$

Lower criterion indicates that a small voltage is applied at the terminal of the switches of the topology.

Tables 4 and 5 compare the power component requirements among the conventional and suggested multilevel inverters for the same number of the output voltage steps, respectively. It is necessary to notice that the number of components is integers. Thus, if an integer number has not been obtained, the nearest integer number is certainly the proposed solution. Figs. 8–10 show the results of the comparison of the conventional and suggested cascaded multilevel inverters from different points of review.

Fig. 8 compares the standing voltage on switches S_1–S_{2n} in suggested topology as shown in Fig. 5 with the conventional topology. This figure shows that the standing voltage on switches S_1–S_{2n} in the suggested topology is less than the conventional topology for realizing N_{step} voltages for output. It is important to mention that the suggested topology needs to four switches (S'_1–S'_4) with the high capability of the standing voltage according to the Table 5.

Fig. 9 compares the number of switches (IGBTs and gate drivers) in the topology recommended in this paper with the conventional topology. As this figure shows, the suggested topology needs fewer switches for realizing N_{step} voltages for output. This point reduces the installation area, the number of the gate driver circuits. Therefore, the cost of the suggested topology is less than the conventional topology for realizing N_{step} voltages for output. It is important to note the number of IGBTs and the main diodes is the same.

One of the important problems for asymmetric multilevel inverters is the variety of the magnitudes of dc voltage sources.

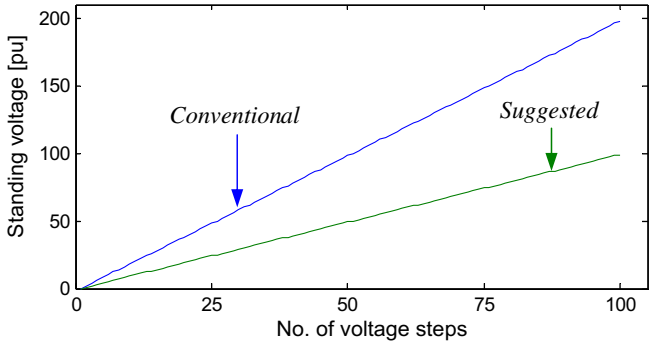
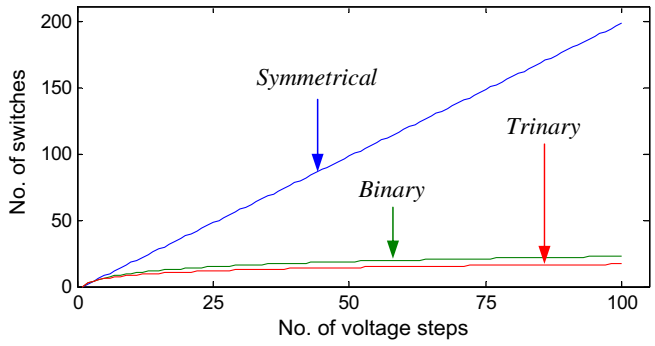
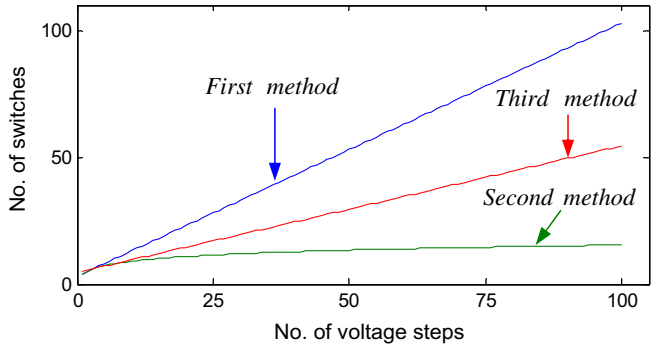


Fig. 8. Comparison of the standing voltage on switches S_1–S_{2n} to realize N_{step} voltages in the suggested structure and conventional cascaded inverter.

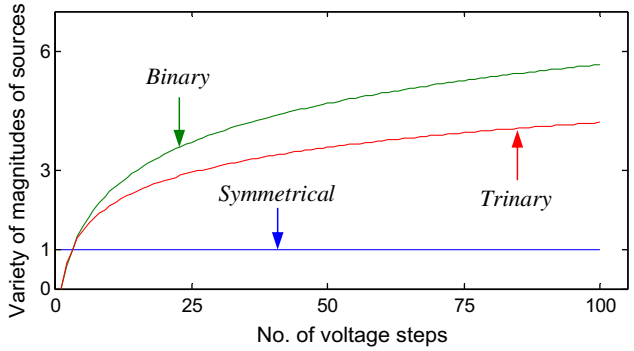


(a) Conventional cascaded inverter

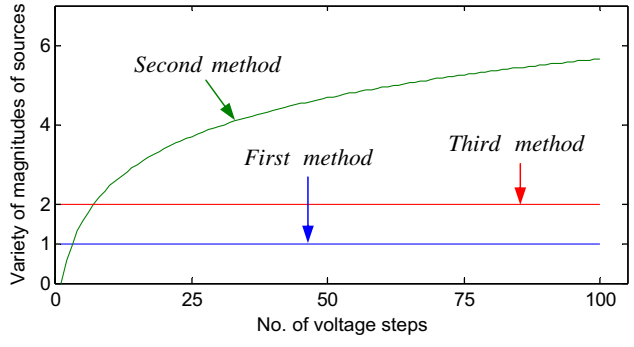


(b) Suggested structure

Fig. 9. Comparison of the required number of switches to realize N_{step} voltages.



(a) Conventional cascaded inverter



(b) Suggested structure

Fig. 10. Comparison of the variety of the magnitudes of dc voltage sources to realize N_{step} voltages.

As Fig. 10 shows, the variety of the magnitudes of dc voltage sources in asymmetric state of the suggested topology (second method) is less than the recommended methods in conventional topology.

6. Simulation and experimental results

To examine the performance of the proposed multilevel inverter in the generation of a desired output voltage waveform, a prototype is simulated and implemented based on the proposed topology according to that one shown in Fig. 11. The PSCAD software has been used for simulation. The multilevel shown in Fig. 11 is a 11-level multilevel inverter and can generate staircase waveform with maximum 100 V on output. The load is a series R–L with magnitudes 70 Ω and 55 mH, respectively.

There are several modulation strategies for multilevel inverters [12,24–28]. In this work, the fundamental frequency switching technique has been used. The benefit of the fundamental frequency switching method is its low switching frequency compared to the other control methods [25]. Table 6 shows the ON switches look-up table and Fig. 12 shows the control block diagram of the inverter. Note that there are different switching patterns for producing the zero level, and in Table 6 only one of them is shown. The main

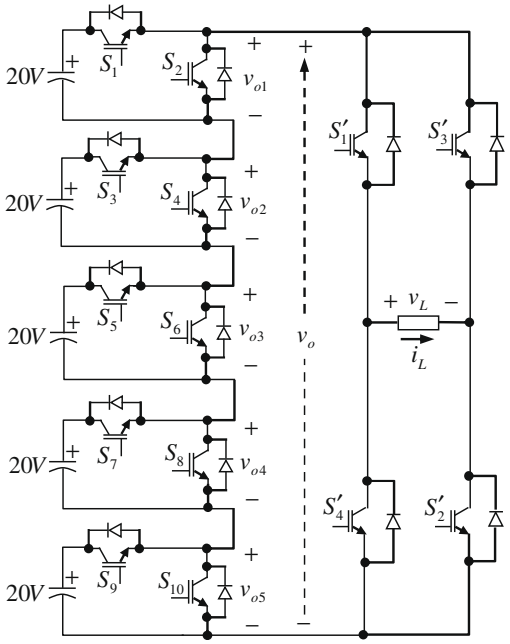


Fig. 11. 11-Level multilevel inverter (according to first method).

Table 6
ON switches look-up table.

$v_L[pu]$ ($20V = 1pu$)	−5	...	−1	0	1	...	5
Switches states							
S_1	On		On	Off	On		On
S_2	Off		Off	Off	Off		Off
S_3	On		Off	Off	Off		On
S_4	Off		On	Off	On		Off
S_5	On		Off	Off	Off		On
S_6	Off		On	Off	On		Off
S_7	On		Off	Off	Off		On
S_8	Off		On	Off	On		Off
S_9	On		Off	Off	Off		On
S_{10}	Off		On	Off	On		Off
S'_1	Off		Off	On	On		On
S'_2	Off		Off	Off	On		On
S'_3	On		On	On	Off		Off
S'_4	On		On	Off	Off		Off

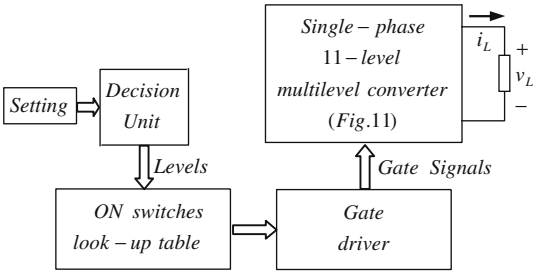


Fig. 12. Control block diagram.

idea in the control strategy is to deliver to the load a voltage that minimizes the error with respect to the reference voltage. It is important to note that the calculation of optimal switching angles for different goals such as elimination of the selected harmonics and minimizing total harmonic distortion (THD) are not the objective of this work.

The IGBTs of the prototype are BUP306D with internal anti-parallel diodes. The 89C52 microcontroller by ATMEL Company has been used to generate the switching patterns.

Fig. 13 shows the measured output voltage waveform. This is a 60 Hz staircase waveform with amplitude 100 V. As it can be seen, the results verify the ability of proposed inverter in generation of desired output voltage waveform.

Figs. 14 and 15 show the simulation results of output voltage and current. Comparing the Figs. 13 and 14 shows the experimental result corresponds very well with the simulation. The Fourier series expansion of the (stepped) output voltages waveform of the multilevel inverter as shown in Fig. 14 is made up from a fundamental frequency sine wave and an infinite number of odd harmonics [29]. As can be seen from the waveforms, the output current is almost sinusoidal. Since the load of the inverters is almost a low pass filter (R–L), then the output currents contain less high order harmonics than the output voltages. For this example, the THDs of the output voltage and current based on simulation are 5.2% and 0.7%, respectively. To generate a desired output with best quality of the waveform, the number of the voltage steps should be increased.

Fig. 16 shows the output voltage of different units. Each unit generates a quasi-square waveform. As this figure shows, the output voltage of each unit for all times has zero or positive values.

Fig. 17 shows input voltage of the full-bridge. As this figure shows the input voltage of the full-bridge has zero or positive values. This is because the ac output of each unit is connected in series

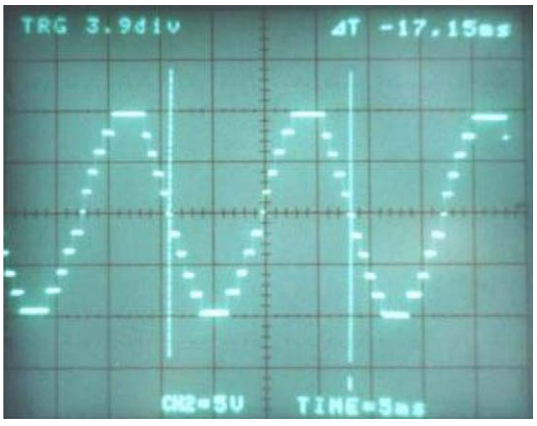


Fig. 13. Measured output voltage (by 10:1 probe) (v_L).

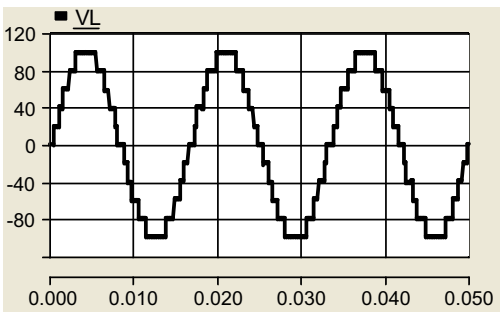


Fig. 14. Simulated output voltage (v_L).

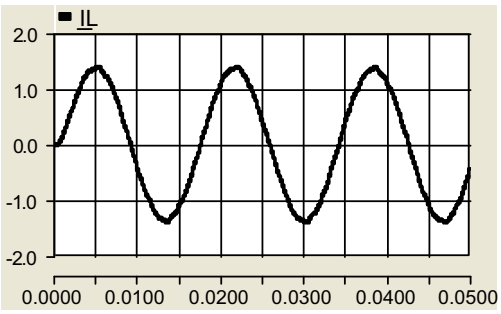


Fig. 15. Output current (i_L).

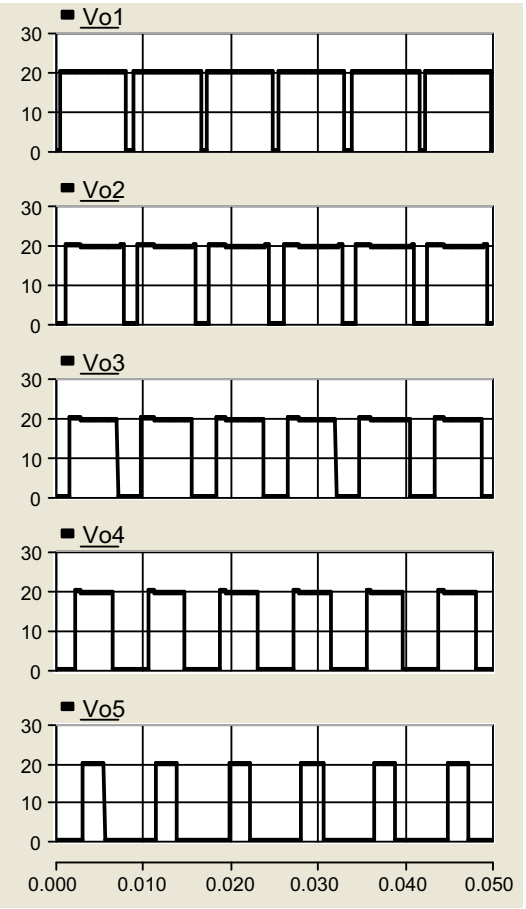


Fig. 16. Output voltage of units.

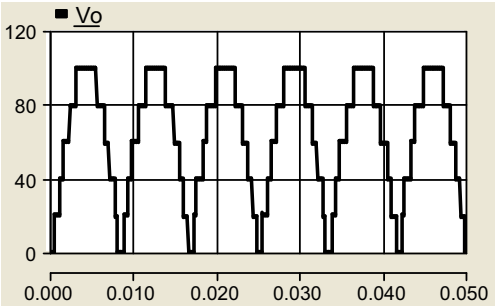


Fig. 17. Input voltage of the full bridge (v_o).

such that the synthesized voltage waveform is the sum of the outputs of the units.

The standing voltages of the switches S_1–S_{10} and the switches of the full-bridge (S'_1–S'_4) in Fig. 11 are 200 V and 400 V, respectively.

7. Conclusions

A new configuration of cascaded multilevel inverter has been proposed. The suggested topology needs fewer switches and gate driver circuits with minimum standing voltage on switches for realizing N_{step} for the load. Therefore, the proposed topology results in reduction of installation area and cost and has simplicity of control system. Also, three procedures have been presented for determination of the magnitudes of the dc voltage sources. The operation and performance of the proposed multilevel inverter has been verified on a single-phase 11-level multilevel inverter prototype.

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